CLAIMS

What is claimed is.

1. A process comprising:

dispensing a polymer stress-relief layer upon a substrate lower surface under conditions to partially embed an electrical first bump disposed upon the lower surface; and

curing the stress-relief layer.

2. The process of claim 1, following curing the stress-relief layer, further including reflowing the electrical first bump.

3. The process of claim 1, wherein dispensing a polymer includes dispensing in a continuous action.

4. The process of claim 1, wherein dispensing the polymer stress-relief layer includes forming a substantially continuous stress-relief layer film between the electrical first bump and an electrical second bump that is spaced apart and adjacent to the electrical first bump.

5. The process of claim 1, wherein dispensing the polymer stress-relief layer includes forming a substantially continuous stress-relief layer film between the electrical first bump and a plurality of electrical subsequent bumps in excess of two, at least one of which is spaced apart and adjacent to the electrical first bump.

6. The process of claim 1, wherein dispensing the polymer stress-relief layer includes ejecting a substantially continuous polymer mass upon the lower surface that includes a ball grid array in excess of four electrical bumps including the electrical first bump.

7. The process of claim 1, wherein dispensing the polymer stress-relief layer includes ejecting a discrete series of quanta of polymer masses upon the lower surface that includes a ball grid array in excess of four electrical bumps including the electrical first bump.

8. The process of claim 1, wherein dispensing the polymer stress-relief layer includes ejecting a polymer first mass and a polymer second mass upon the lower surface that includes a ball grid array of at least six electrical bumps:

wherein the electrical first bump is in a rectangular pattern with an electrical second bump, an electrical third bump, and an electrical fourth bump, wherein the polymer first mass is ejected contiguous with only the electrical first bump, the electrical second bump, the electrical third bump, and the electrical fourth bump; and

wherein the electrical first bump and the electrical second bump are in a rectangular pattern with an electrical fifth bump and an electrical sixth bump, wherein the polymer second mass is ejected contiguous with only the electrical first bump, the electrical second bump, the electrical fifth bump, and the electrical sixth bump.

9. The process of claim 1, wherein the electrical first bump includes a first height, and wherein dispensing the polymer stress-relief layer includes dispensing in a depth range against the electrical first bump in a range from about 5 percent the first height to about 95 percent the first height.

10. An article comprising:

a mounting substrate including a lower and an upper surface;

an electrical first bump disposed on the lower surface;

a stress-relief layer disposed on the lower surface, wherein the electrical first bump is at least partially embedded in the stress-relief layer, and wherein at least a portion of the electrical first bump is exposed below the stress-relief layer; and

a die disposed upon the upper surface that is coupled to the electrical first bump.

11. The article of claim 10, wherein the stress-relief layer includes an organic material.

12. The article of claim 10, wherein the stress-relief layer includes an organic material, and wherein the organic material includes a filler particulate.

13. The article of claim 10, wherein the stress-relief layer includes a first stress-relief layer, wherein the first stress-relief layer is disposed between the electrical first bump, an electrical second bump that is spaced apart and adjacent to the electrical first bump, an electrical third bump that is spaced apart and adjacent to the electrical first bump, and an electrical fourth bump that is spaced apart and adjacent to the electrical first bump, the stress-relief layer further including:

a second stress-relief layer disposed between the electrical first bump and an electrical fifth bump that is spaced apart and adjacent to the electrical first bump.

14. The article of claim 10, wherein the electrical first bump is in a rectangular pattern with an electrical second bump, an electrical third bump, and an electrical fourth bump, and wherein the stress-relief layer is disposed in about the geometric center of the rectangular pattern.

15. The article of claim 10, wherein the electrical first bump is in a rectangular pattern with an electrical second bump, an electrical third bump, and an electrical fourth bump, and wherein the stress-relief layer is disposed contiguous with only the electrical first bump, the electrical second bump, the electrical third bump, and the electrical fourth bump.

16. The article of claim 10, wherein the polymer stress-relief layer includes a polymer first mass and a polymer second mass disposed upon the lower surface that includes a ball grid array of at least six electrical bumps:

wherein the electrical first bump is in a rectangular pattern with an electrical second bump, an electrical third bump, and an electrical fourth bump, wherein the polymer first mass is contiguous with only the electrical first bump, the electrical second bump, the electrical third bump, and the electrical fourth bump; and

wherein the electrical first bump and the electrical second bump are in a rectangular pattern with an electrical fifth bump and an electrical sixth bump, wherein the polymer second mass is contiguous with only the electrical first bump, the electrical second bump, the electrical fifth bump, and the electrical sixth bump.

17. The article of claim 10, wherein the electrical first bump includes a first height, and wherein the polymer stress-relief layer includes a depth range against the electrical first bump in a range from about 5 percent the first height to about 95 percent the first height.

18. A package comprising:

a board including a bottom and a land side;

a substrate including a lower surface and an upper surface, wherein the board is disposed on the substrate land side;

a solder first bump disposed on the lower surface;

a stress-relief layer disposed on the lower surface, wherein the solder first bump is at least partially embedded in the stress-relief layer, and wherein at least a portion of the solder first bump is exposed above the stress-relief layer; and

a die dispose upon the upper surface.

19. The package of claim 18, wherein the stress-relief layer is a first stress-relief layer, wherein the first stress-relief layer is disposed between the solder first bump and a solder second bump that is spaced apart and adjacent to the solder first bump, the package further including:

a second stress-relief layer disposed between the solder first bump and a solder third bump that is spaced apart and adjacent to the solder first bump.

20. The package of claim 18, wherein the solder first bump is in a rectangular pattern with a solder second bump, a solder third bump, and a solder fourth bump, and wherein the stress-relief layer is disposed in about the geometric center of the rectangular pattern.

21. The package of claim 18, wherein the solder first bump is in a rectangular pattern with a solder second bump, a solder third bump, and a solder fourth bump, and wherein the stress-relief layer is disposed contiguous with only the solder first bump, the solder second bump, the solder third bump, and the solder fourth bump.

22. The package of claim 18, wherein the polymer stress-relief layer includes a polymer first mass and a polymer second mass disposed upon the lower surface that includes a ball grid array of at least six solder bumps:

wherein the solder first bump is in a rectangular pattern with a solder second bump, a solder third bump, and a solder fourth bump, wherein the polymer first mass is contiguous with only the solder first bump, the solder second bump, the solder third bump, and the solder fourth bump; and

wherein the solder first bump and the solder second bump are in a rectangular pattern with a solder fifth bump and a solder sixth bump, wherein the polymer second mass is contiguous with only the solder first bump, the solder second bump, the solder fifth bump, and the solder sixth bump.

23. The package of claim 18, wherein the solder first bump includes a first height, and wherein the polymer stress-relief layer includes a depth range against the solder first bump in a range from about 5 percent the first height to about 95 percent the first height.

24. A computing system comprising:

a microelectronic die;

a mounting substrate including a lower and an upper surface;

a solder first bump disposed on the lower surface;

a stress-relief layer disposed on the lower surface, wherein the solder first bump is at least partially embedded in the stress-relief layer, and wherein at least a portion of the solder first bump is exposed above the stress-relief layer;

a die disposed upon the upper surface and coupled to the solder first bump; and

at least one of an input device and an output device coupled to the solder first bump.

25. The computing system of claim 24, wherein the computing system is disposed in one of a computer, a wireless communicator, a hand-held device, an automobile, a locomotive, an aircraft, a watercraft, and a spacecraft.

26. The computing system of claim 24, wherein the die is selected from a data storage device, a digital signal processor, a micro controller, an application specific integrated circuit, and a microprocessor.